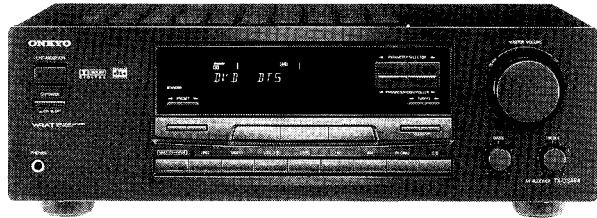
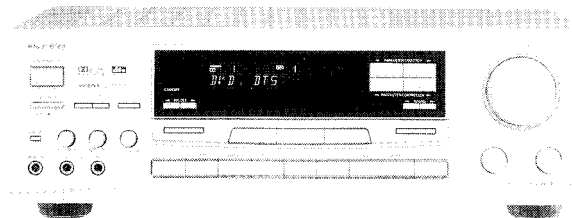


ONKYO® SERVICE MANUAL

AUDIO VIDEO RECEIVER MODEL TX-DS484



AUDIO VIDEO KARAOKE RECEIVER MODEL TX-SE570



Black, Silver, and Golden models

BMD	120V AC, 60Hz
GMGK	220V AC, 60Hz
BMP, SMP, BMPT, BMPA	230V AC, 50Hz
GMWT, BMWT, GMWR, BMWR	120/220V AC, 50/60Hz

Black and Golden models

BMWR, GMWR	120/220V AC, 50/60Hz
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SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK Δ ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PARTS NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

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MICROPROCESSOR-TERMINAL DESCRIPTION

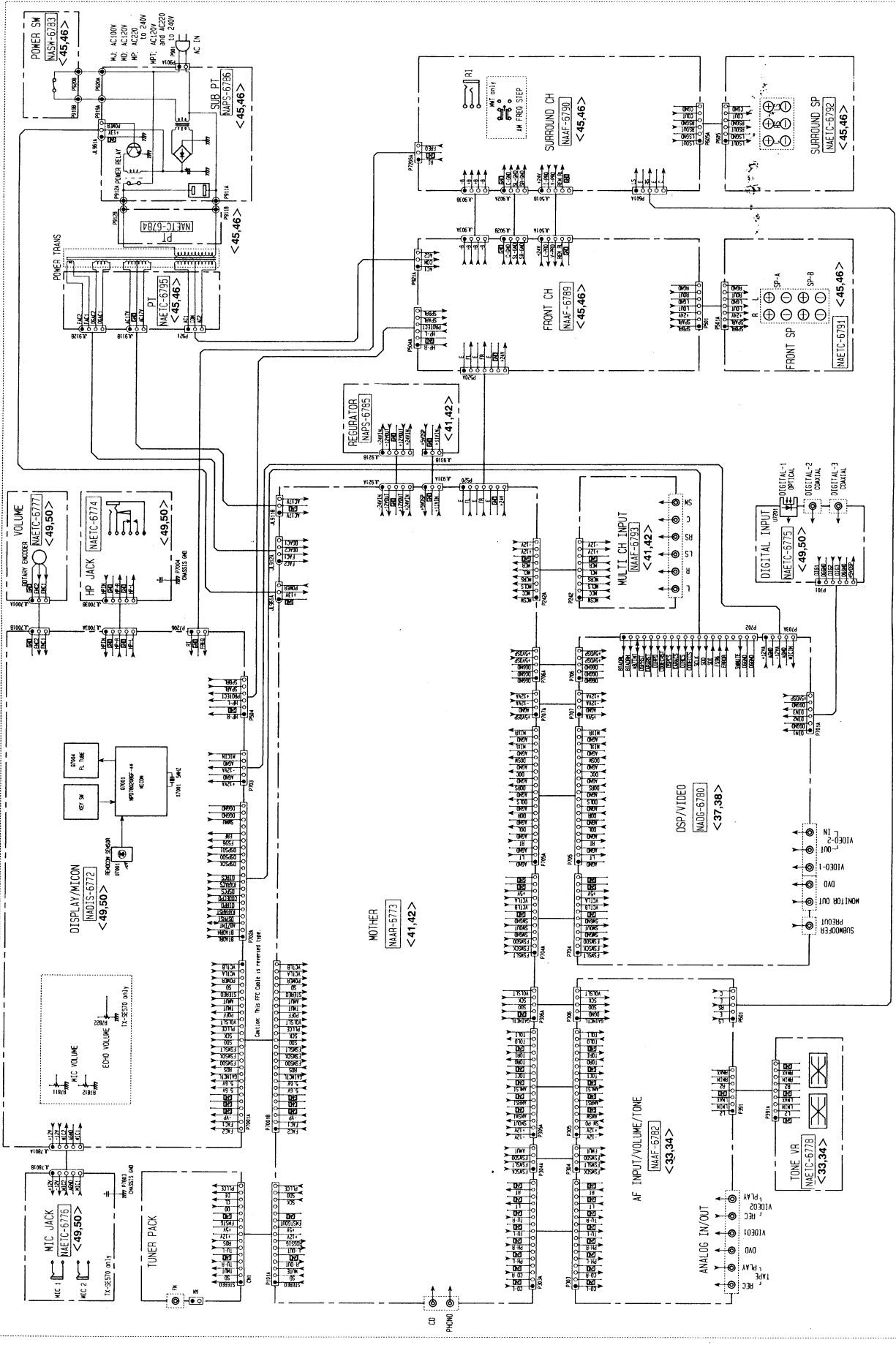
MODEL TX-DS484

Q7001: μ PD780208GF

No.	Function	I/O	Description	No.	Function	I/O	Description
1	VDD	1	Power supply terminal (+5V)	38	RDSSCK	1	Clock input terminal from RDS decoder.
2	STANDBY/RECV	0	STANDBY/RECEIVED inductor control output terminal.	39	REMIN	1	Signal input terminal from remote sensor.
3	FSWSDO	0	Data output terminal to function switch ICs.	40	VSS	1	Power supply terminal (GND).
4	FSWSCK	0	Clock output terminal to function switch ICs.	41	TUMUT	0	Muting control output terminal for tuner section.
5	FSWSLT	0	Latch output terminal to function switch ICs.	42	AMUT	0	Muting control output terminal for amplifier section.
6	RDSDATA	1	Data input terminal from RDS decoder.	43	ABOOTH/INT	I/O	AUTOBOOT and INTREQ I/O terminal for DSP(CS4296).
7	SDO	0	Data output terminal to PLL IC and Master volume IC(TC9482N).	44	KARRST	0	Not used.
8	SCK	0	Clock output terminal to PLL IC and Master volume IC(TC9482N).	45	CFGAIN	0	Not used.
9	PLICE	0	Chip enable output terminal to PLL IC.	46	VDD	1	Power supply terminal (+5V).
10	RESET	1	System reset input terminal.	47	GAINCTL	0	Gain control output terminal.
11	X1	0	Ceramic oscillator connection terminals.	48	CODECPD	0	Power down signal output terminal to CODEC(AK4526).
12	X2	0	Connect 5.0MHz ceramic oscillator between the both terminals.	49	DIRPD	0	Power down signal output terminal to DIR (AK4110).
13	GND	1	Internal connection terminal (to GND)	50	DIRCS	0	Chip enable output terminal to DIR (AK4110).
14	X12	0	Sub-system clock output terminal. Not used.	51	BTADR1	0	Output terminal to set LSB position of address to boot ROM(1C372100).
15	X11	1	Sub-system clock input terminal. Not used.(to GND)	52	BTADRH	0	Output terminal to set MSB position of address to boot ROM(1C372100).
16	Vdd	1	Power supply terminal (+5V)	53	SD	1	Broadcast detection input terminal.
17	VOL_SLT	0	Latch output terminal to Master volume IC(TC9482N).	54	STEREO	1	Stereo broadcast detection input terminal.
18	SYSDOUT	0	System code output terminal.	55	RDSSIG	1	Signal input terminal from RDS decoder.
19	DSPSDI	1	Data input terminal from DIR(AK4110).	56	SWMUTE	0	SW Preout muting control output terminal for amplifier section.
20	DSPSDO	0	Data output terminal to DIR (AK4110).DSPCS4926.)	57	ERF	1	ERF Signal input terminal from DIR(AK4110).
21	DSPSCK	0	Clock output terminal to DIR (AK4110).DSPCS4926)	58	FS96	0	FS96 Signal output terminal to CODEC(AK4526)
22	KARCS	0	Not used.	59	CODECS	0	Not used.
23	DSPCS	0	Chip enable output terminal to DSPCS4926).	60	ENC1	1	Volume control input terminal.
24	DSPRST	0	Reset output terminal to DSP(CS4926).	61	ENC2	1	Volume control input terminal.
25	AVSS	1	Power supply terminal (GND)	62	PROTECT	1	Detection input terminal for protection circuit.
26	AMPK/10K	1	Initializing input terminal for AM band step.	63	POWER	0	Relay control output terminal for power.
27	HPIN	1	Input terminal when the headphone is inserted.	64	VCTLB	0	Video selector control output terminal.
28	MODE	1	Initializing input terminal of operation mode..	65	VCTLA	0	Video selector control output terminal.
29	ECHO	1	Not used.	66	SPARL	0	Control output terminal for SPEAKER A relay.
30~33	K3~K0	1	Operation key connection terminals.	67	SPBRL	0	Control output terminal for SPEAKER B relay.
34	AVDD	1	Power supply terminal (+5V)	68~78	P17~P7	0	Segment output terminals for FL tube.
35	AVREF	1	Reference voltage terminal.	79	VLOAD		Power supply terminal for FL tube.
36	SVSIN	1	System code input terminal.	80~85	P6~P1	0	Segment output terminals for FL tube.
37	POFF	1	Power failure's detection terminal.	86~100	15G~1G	0	Grid output terminals for FL tube.

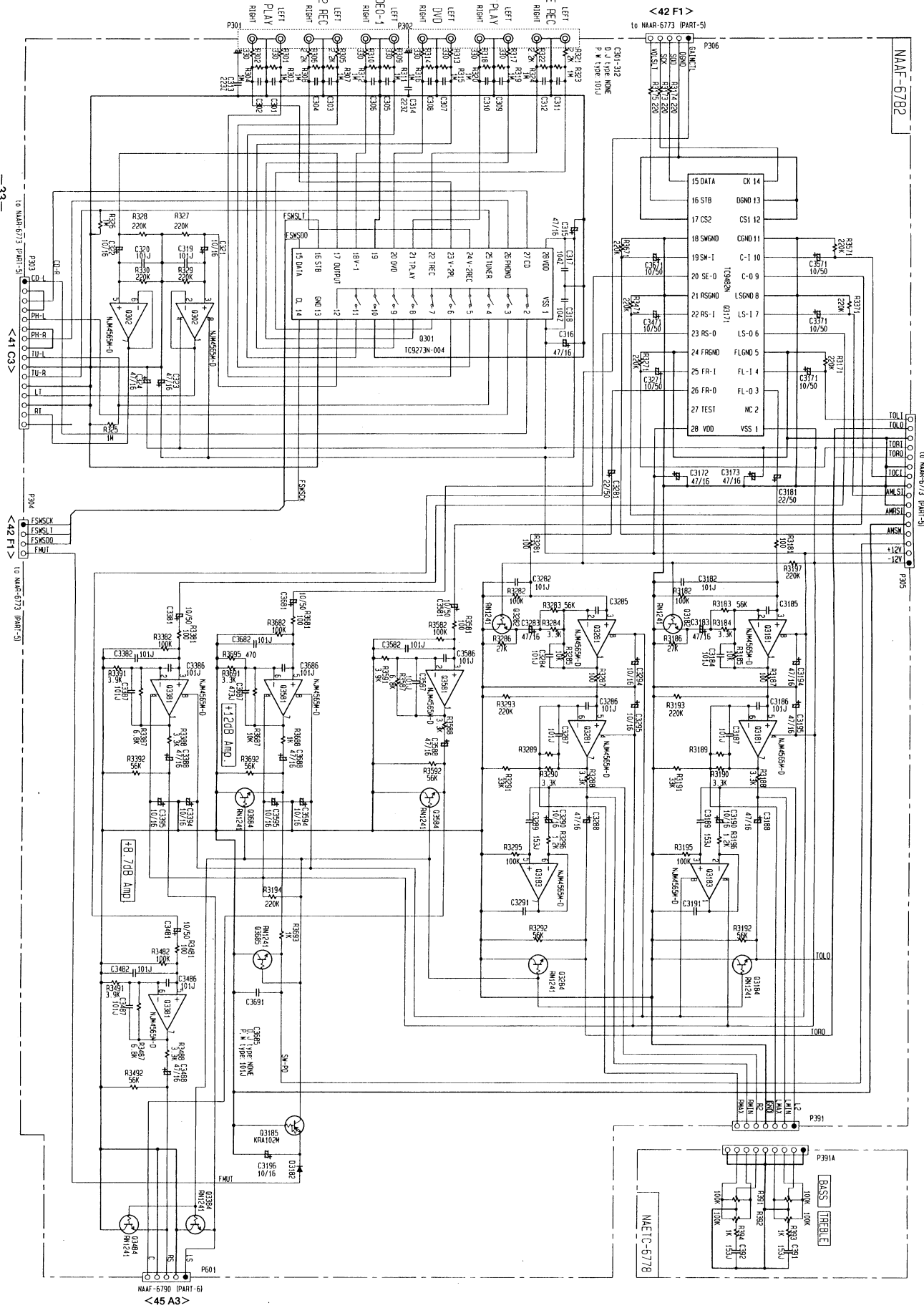
WIRING BOARD DIAGRAM

Note: For the information about schematic diagram, refer to the pages listed in the brackets < >



SCHEMATIC DIAGRAM

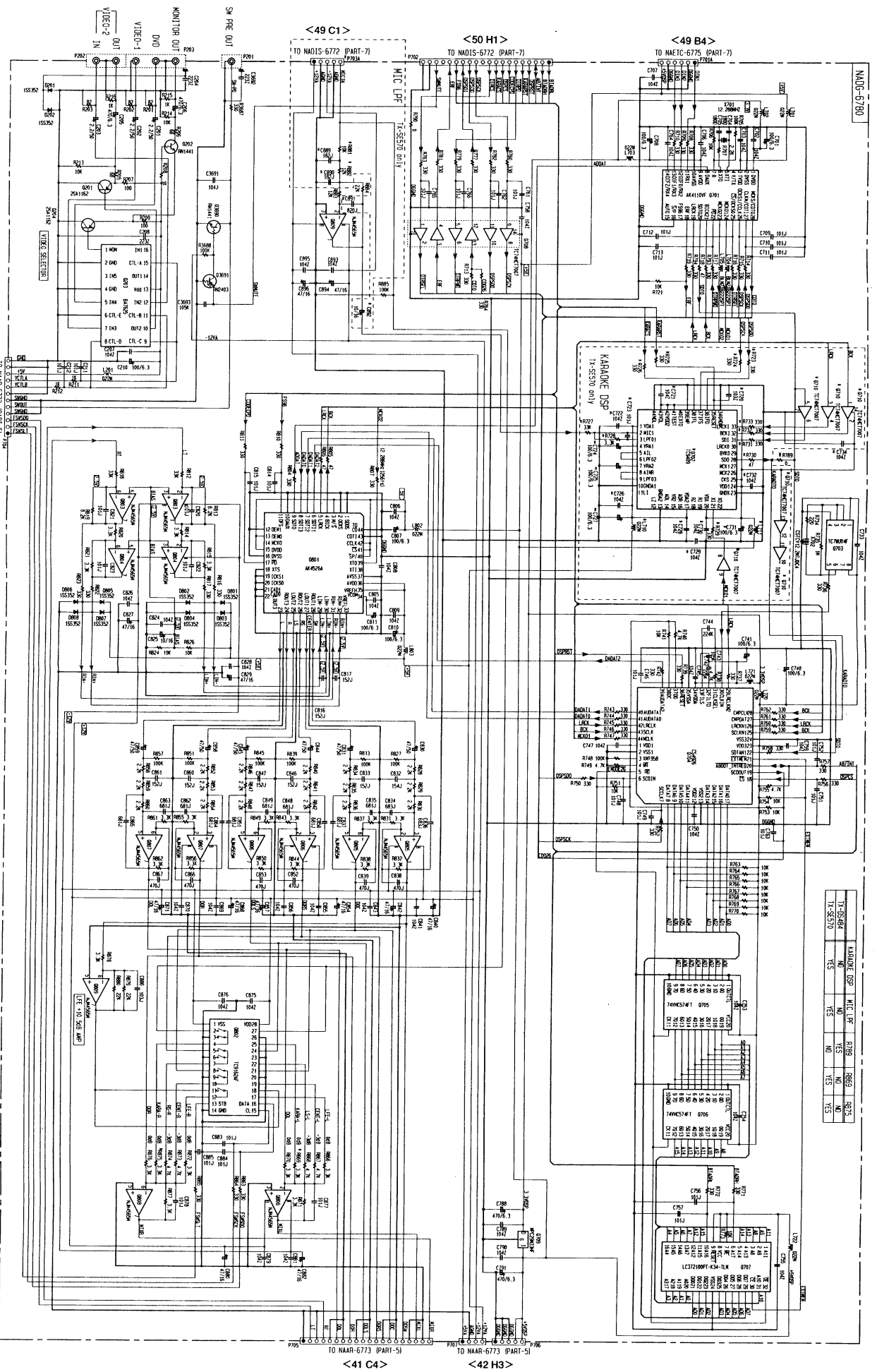
A B C D E F G H



1 2 3 4 5

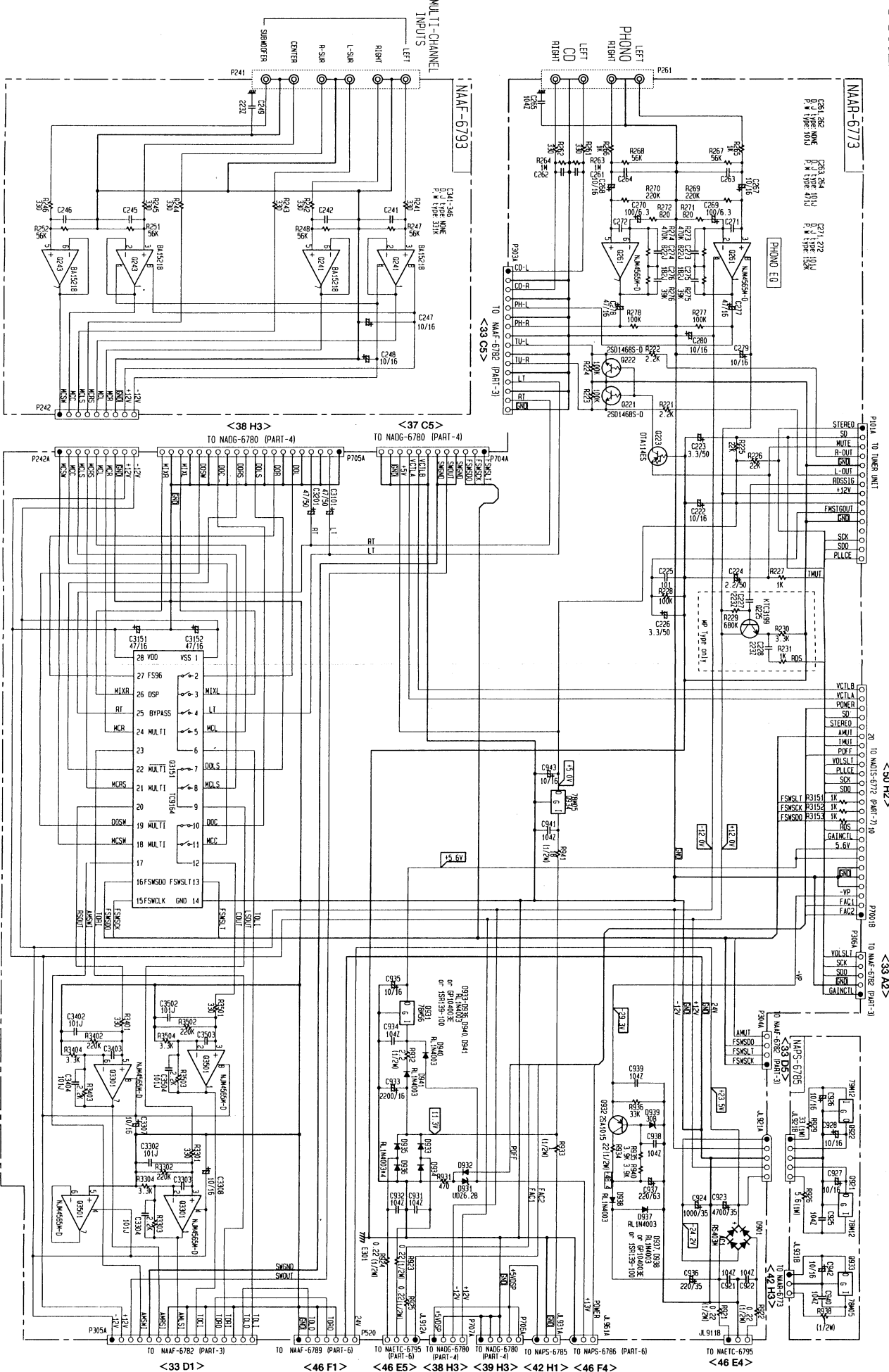
SCHEMATIC DIAGRAM

A B C D E F G H



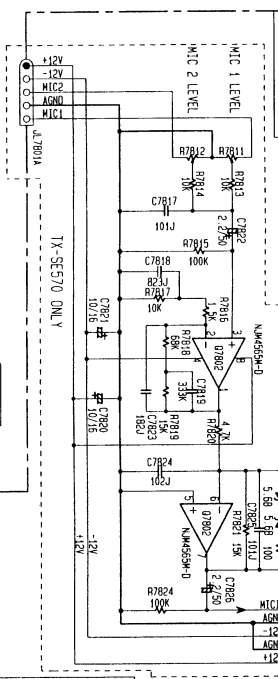
IC	DESCRIPTION	QTY	REF. DESIG.	QTY	REF. DESIG.
IC10	KARAOKE DSP	1	7199	5000	9275
IC11	MIC LPF	1	715	40	40
IC12	KARAOKE AMP	1	715	131	715

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM

NAID-6772



<37 A4>

